The Model 765 Pulse Generator

Application Note: Semiconductor

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Non-Volatile Memory Cells Characterization

The trend of memory research is to develop a new memory called Non-Volatile RAM that joins the speed of RAM with the data retention of mass memory.

There are many proposals of new cell types. For example: FeRAM (Ferroelectric RAM), ReRAM (Resistive RAM), MRAM (Magnetoresistive RAM), STT- MRAM (Spin-Transfer Torque Magnetoresistive RAM) and PCM (Phase Change Memory).

Those types of memories are based on the changing of conductivity of a material using a different physical principle (for example, formation and destruction of a thin wire into a material stack, or the change of the material structure from amorphous to polycrystalline, or the alignment of the magnetic field).

This application note will describe how to test an STT-MRAM cell using a pulse generator.

MRAM memory cells use Magnetic Tunnel Junctions (MTJ) that consist of two ferromagnets separated by a thin insulator. If the magnetic fields of the two ferromagnets are oriented in the same direction, electrons can tunnel from one ferromagnet to the other through an insulator layer. The first ferromagnet has a fixed magnetic field, while the field of the second one can be changed by applying a current pulse to invert the magnetic field orientation which changes the conductivity of the stack.

To program or erase a bit, a current pulse is applied through the stack; the assumed orientation of magnetic field depends on the current pulse direction.

The efficiency of the program-and-erase process depends on the duration and amplitude of the pulse, so during research and development stages on this technology, it can be useful to test different combinations of pulse width and amplitude. A simple way to do this is to use a pulse generator that allows the user to change the width, amplitude and repetition rate.

Figure 1: Model 765 setup to program or erase a single cell: pulse characteristics: 50 ns @ 3.3V

Figure 2: Model 765 setup to program or erase an array of cells: pulse characteristics: 100 ns @ 3.3V

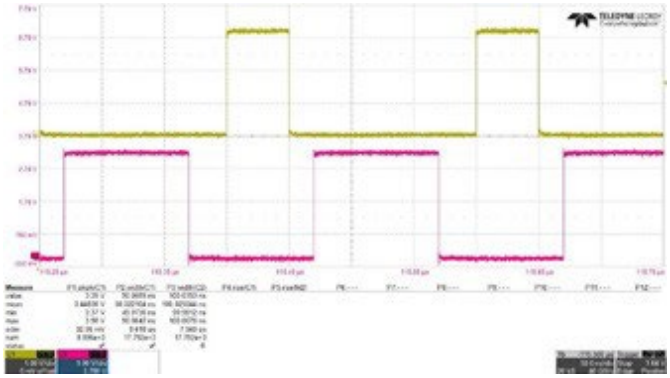
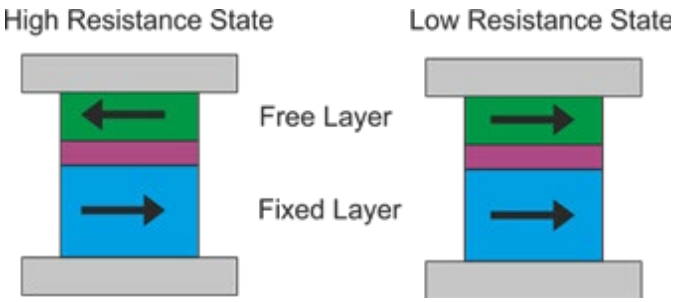


Figure 3: In this example, the pulse generator supplies pulses of 50 ns @ 3.3 V to simulate the program or erase a cell. On the second channel it supplies 100 ns @ 3.3 V to program or erase of a cell array.



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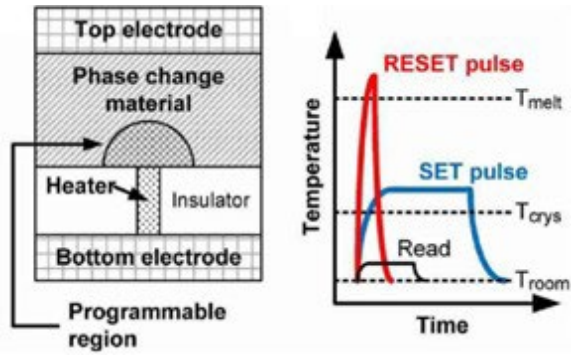
PCM memory cell is based on amorphous-to-crystalline phase changing of chalcogenide material. When the material is in amorphous phase the resistance is high and when it is in crystalline phase the resistance is lower.

To program or erase a bit, it is necessary to change the phase of the material: a large but low voltage pulse changes the phase from amorphous to crystalline, whereas, a short but higher voltage pulse changes the phase from crystalline to amorphous.



As shown in the image, the control of the amplitude and width of pulses is fundamental. The Model 765 pulse generators offer a time resolution of 10 ps and a vertical resolution of 10 mV.

Newer technologies applied on the Non-Volatile RAM require faster pulses every day. The Model 765, with transition time under 70 ps and an amplitude up to 5 Vpp, is the perfect choice for such requirements.

Figure 4: Model 765 setup for a narrow pulse 10ns @ 3.3V (Reset Pulse)

Figure 5: Model 765 setup for a “large” pulse 80ns @ 1.6 V (Set Pulse)

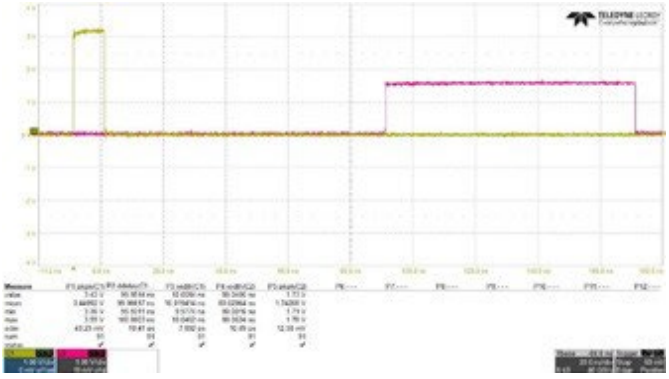


Figure 6: In this example, the pulse generator supplies pulses of 10 ns @ 3.3 V and 80 ns @ 1.6 V to simulate the erasing and programming of a cell.

MOSFET Test

In the development of the modern MOSFET transistor, the challenge is to use high $_K$ material for the dielectric in the MOS capacitor. This gives the advantage of reduced leakage current through the isolator but at the same time, it causes problems due to charge trapping, like voltage threshold instability, carrier channel mobility degradation, and reduction of reliability.

Charge trapping occurs when the transistor is in the “on” state and a bit of channel charge is accumulated into an isolation layer creating a built-in potential that changes the threshold.

The charge trapping phenomena depends on various physical parameters of the gate stack such as the thickness, type of dielectric, and technology process, but it also depends on gate voltage and pulse duty cycle.

It is very important to understand the charge trapping mechanism to improve this technology.

The order of magnitude of this phenomenon varies from under 1 µs to dozens of milliseconds so the DC

measurements are unreliable, therefore different types of pulsed I-V measurements are used.

All types of I_d V_g measurements are obtained biasing the drain terminal and supplying pulses into the gate terminal. Depending on the type of pulse, it is possible to divide the measurements into 3 main categories:

- DC I_d V_g curves: Gate signal is a DC level. By repeating the measurement for many bias points, the curve is achieved. In this way, the results depend on the charge trapping effects due to the biasing. This measurement isn't reliable for devices developed to switch at a high rate.

- Short Pulse I_d V_g curves: By supplying pulses with fast edges and a width in the order of nanoseconds, it is possible to analyze the response of an intrinsic device, because the charge doesn't have time to accumulate into a dielectric layer. Finally, repeating the measurement for different bias points is possible to obtain the curve. This measurement doesn't give information about the charge trapping phenomenon.

- Slow Pulse I_d V_g curves: This technique supplies only a long pulse (in the order of microseconds) with ramped edges. In this way, if the ramp is fast enough, the result is representative of the I_d V_g curve of the device because the charge doesn't have time to accumulate in the MOS stack.

The long pulse is required to measure the drain current degradation over time and then observe the trapping charge effect. If the goal is to study the charge trapping effect at a defined bias point, the slew rate of the edges does not matter but it is important that the rising edge is very fast.

If the edges are fast enough, the obtained results are directly comparable to both DC and Short Pulse curves for that bias point because immediately after the leading edge of the gate voltage, the drain current is comparable to that obtained from pulsed measurements. Then the drain current starts to decrease over time until it arrives at the value measured through DC measurements.

The Slow Pulse technique can also be used to predict the lifetime of devices developed for switching by studying the increment of charge trapping effects before, and after switching stress.

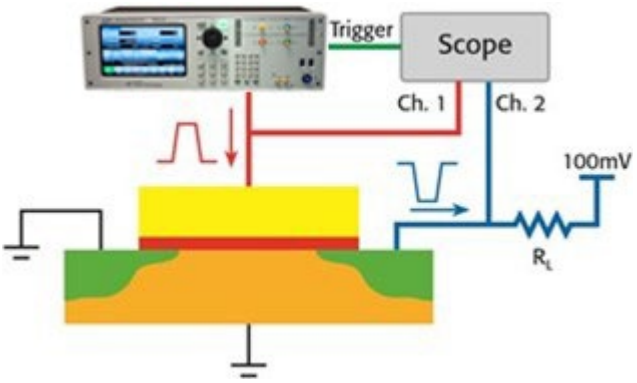


Figure 7: Principle scheme of a set-up for the I_d V_g measurement

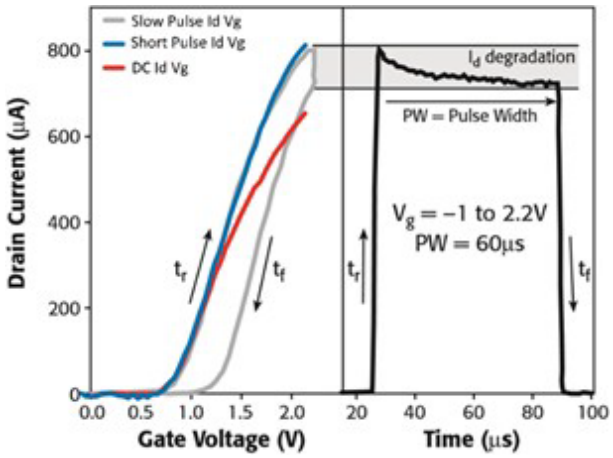


Figure 8: Example of comparison among the different measurement solutions

The Model 765 pulse generator supplies fast edges under 70 ps, an amplitude up to 5 Vpp, a baseline offset of +-2.5 V, and a pulse width from 300 ps up to 1 s, so it may be the ideal instrument to generate the pulses for Short and Slow Pulse tests.

Figure 9: Screen UI "short pulse" baseline -1V, max 2V2 (amplitude 3.2V) duration 30 ns single mode

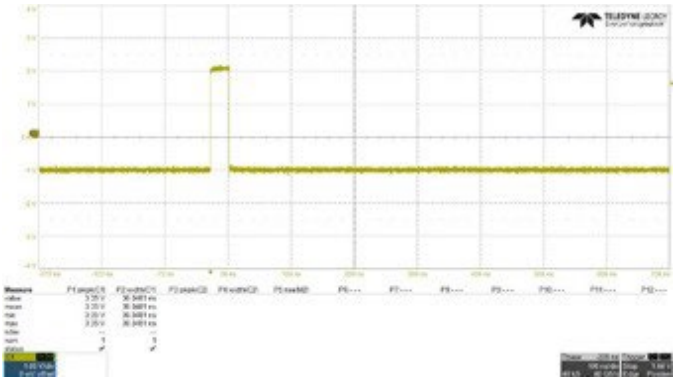


Figure 10: Oscilloscope screenshot of gate pulse for short pulse MOSFET characterization

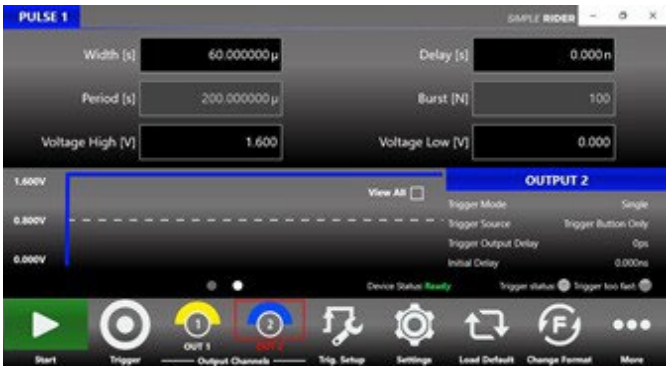


Figure 11: Screen UI “slow pulse” baseline -1V, max 2V2 (amplitude 3,2V) duration 60 us single mode

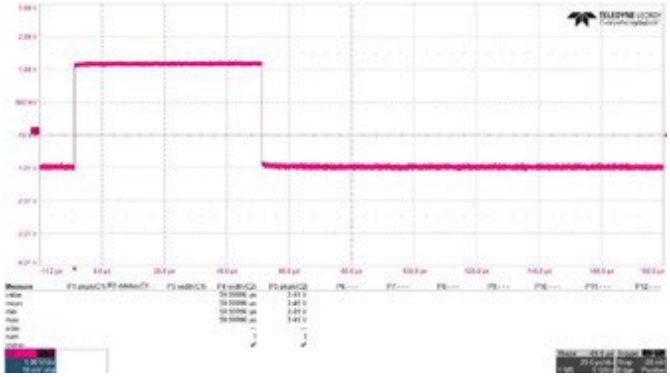


Figure 12: Oscilloscope screenshot of gate pulse for spct MOSFET characterization

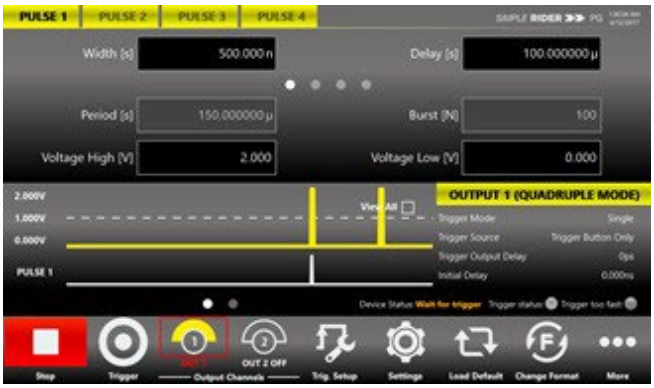


Figure 13: Model 765 interface waiting with quadruple pulse setting

About Berkeley Nucleonics Corporation

Berkeley Nucleonics Corporation (BNC) is a leading manufacturer of precision electronic instrumentation for test, measurement, and nuclear research. Our corporate headquarters are in San Rafael, California, with additional manufacturing facilities and sales offices located throughout

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